Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 42501

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018

Fourth Semester

Electrical and Electronics Engineering

EE 2255 – DIGITAL LOGIC CIRCUITS

(Regulations 2008)

(Common to PTEE 2255 – Digital Logic Circuits for B.E. (Part-Time) Third Semester – EEE – Regulations 2009)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. State the associative property of Boolean algebra.
2. Reduce A(A + B).
3. Define duality property.
4. What is a Karnaugh map ?
5. What is a master-slave flip-flop ?
6. Give the comparison between synchronous and Asynchronous counters.
7. Define address and word.
8. Why was PAL developed ?
9. Define Cache Memory.
10. Infer the concept of Switch-level modeling.

PART – B **(5×16=80 Marks)**

11. a) i) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC. **(10)**

ii) Convert the given expression in canonical SOP form Y = AC + AB + BC. **(6)**

(OR)

b) Designing a 4-bit Adder-Subtractor Circuit.

12. a) Write down the steps in implementing a Boolean function with levels of AND Gates.

(OR)

b) Give the general procedure for converting a Boolean expression into multilevel NAND diagram.

13. a) Explain the operation of SR flip-flop, T flip-flop and JK flip-flop.

(OR)

b) Explain the flip-flop excitation tables for JK flip-flop and RS flip-flop.

14. a) Elaborate the concept of PROM, EPROM, EEPROM in detail.

(OR)

b) Explain the operation of bipolar Ram cell with suitable diagram.

15. a) Give the different arithmetic operators and bitwise operators.

(OR)

b) Explain in detail about the principal of operation of RTL design.
